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(54) **Self-bootstrapping memory device**

(57) A self-bootstrapping device for bootstrapping the bias applied to the gate of a MOS transistor in a decoder (20) of a semiconductor memory device requires a high degree of integration so that the MOS transistor can transmit the potential from its drain to its source. The self-bootstrapping device comprises a first NMOS transistor (Q2) for signal transmission, and a second NMOS transistor (Q3) connected between the gate of the first NMOS transistor and an address decoder circuit (20). The second NMOS transistor (Q3) has a source voltage applied at its gate and comprises first and second diffusion regions (40, 50) formed in a semiconductor substrate and spaced apart a predetermined distance. A gate electrode (60) is formed on the semiconductor substrate between the first and second diffusion regions. In one implementation, the gate electrode (60) and the two diffusion regions (40, 50) are rectangular or annular in shape. The diffusion regions may be of different types, ie N^+ and N^- (figs 6 and 7).

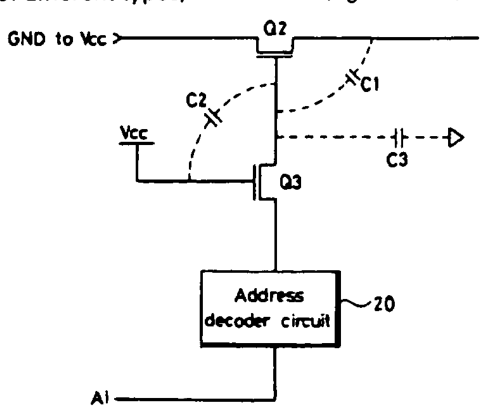

Fig. 2

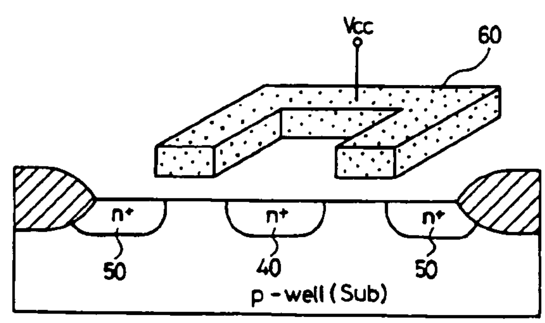

Fig. 5

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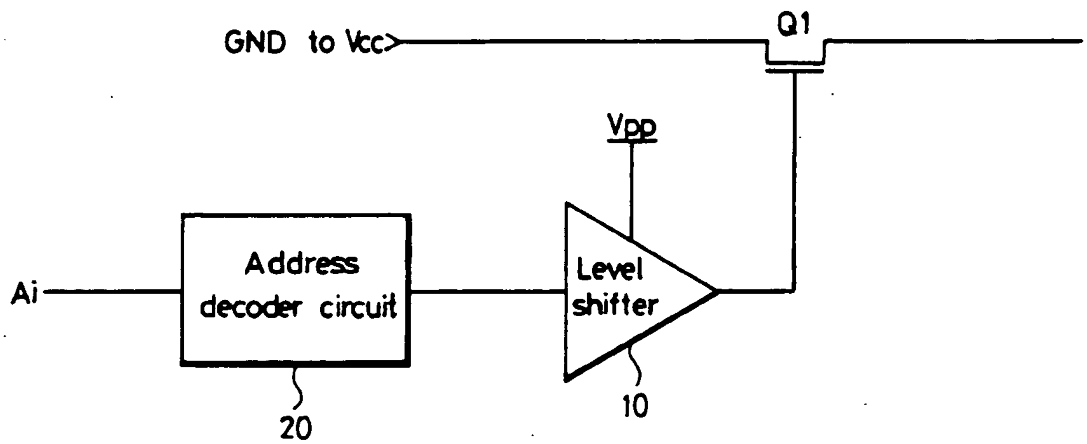
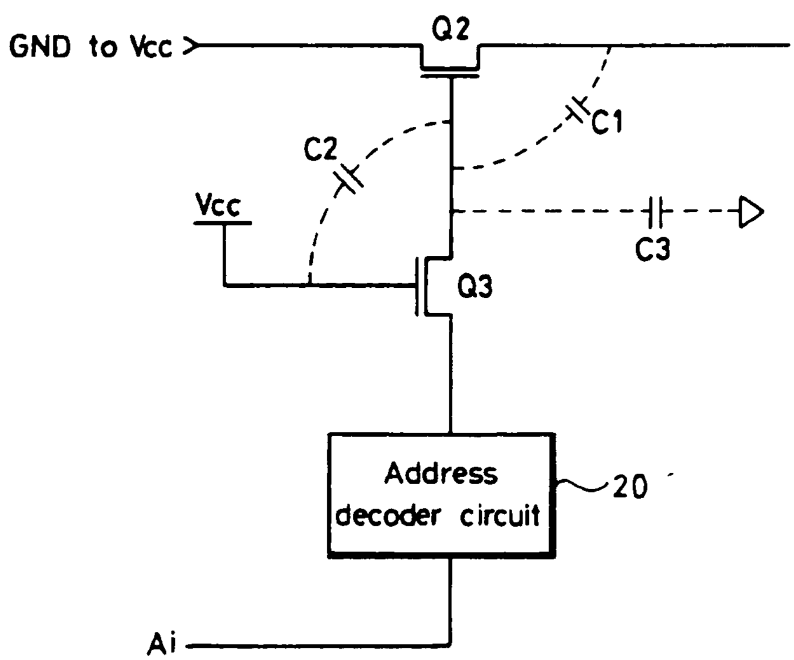


GND to Vcc
Q1
Vpp
Address decoder circuit
Level shifter
Ai
20
10

Fig. 1



GND to Vcc
Q2
C1
C2
Vcc
C3
Q3
Address decoder circuit
20
Ai

Fig. 2

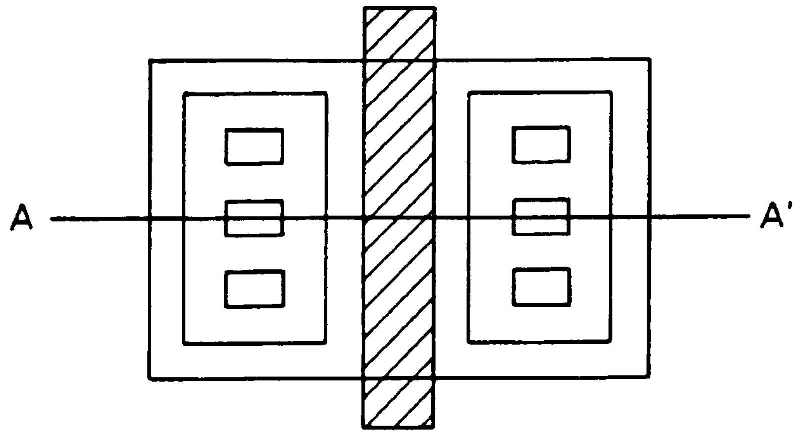


Fig. 3A

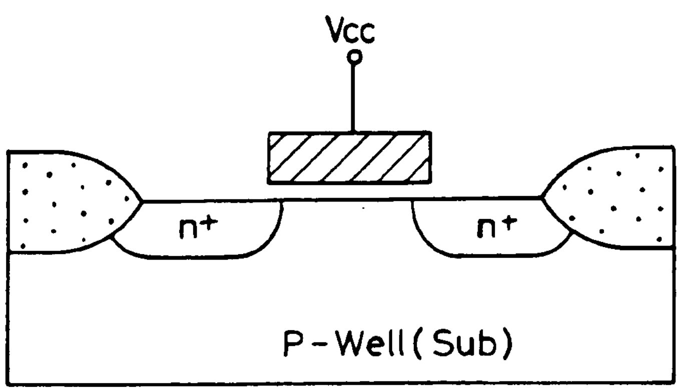


Fig. 3B

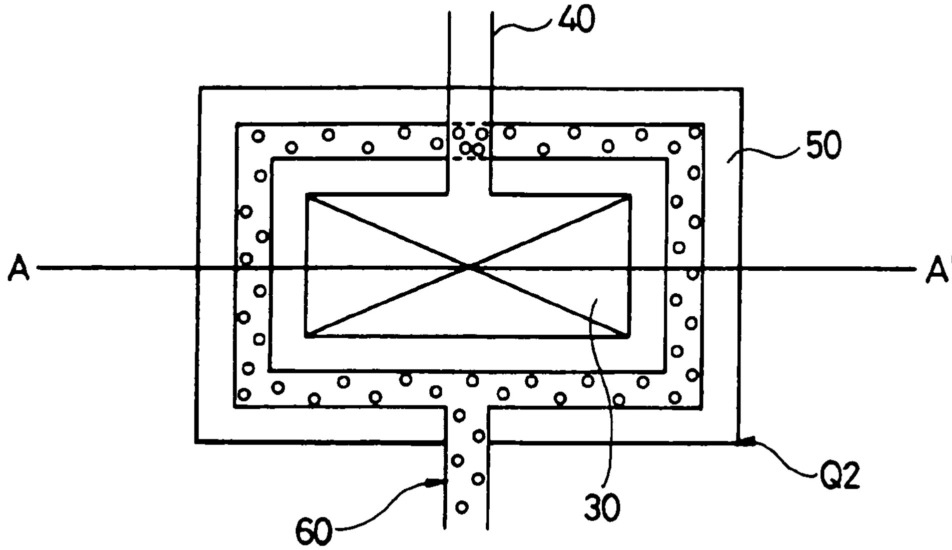


Fig. 4

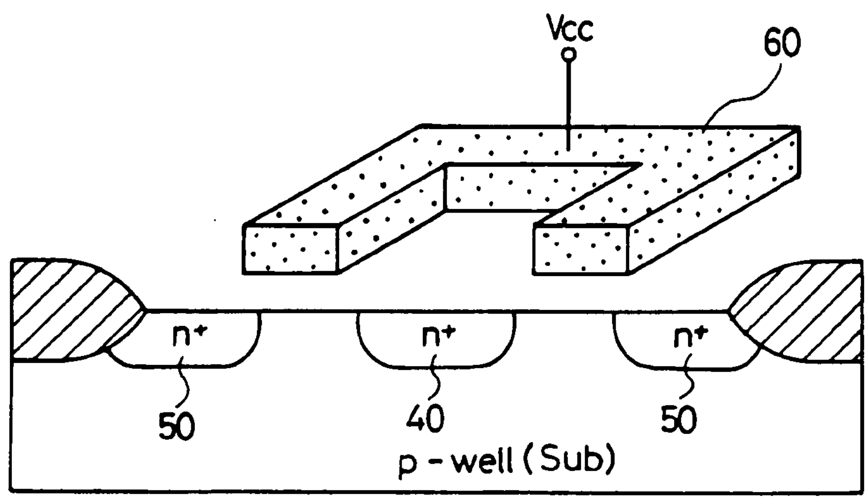


Fig. 5

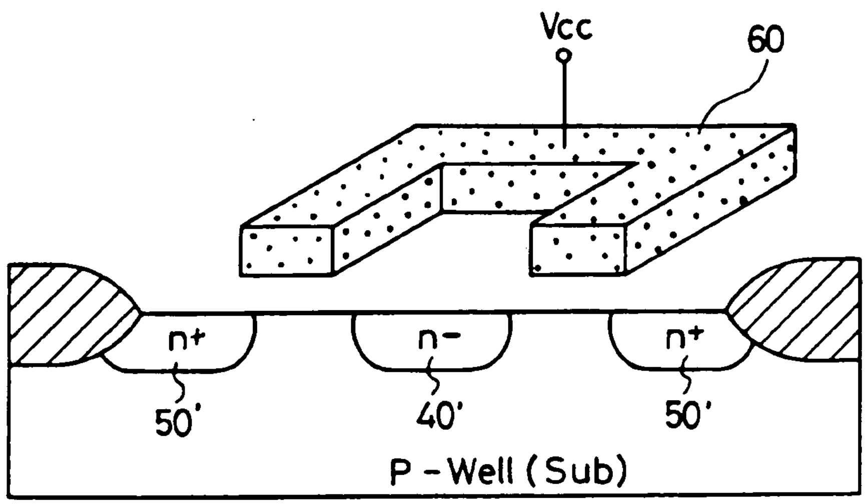


Fig. 6

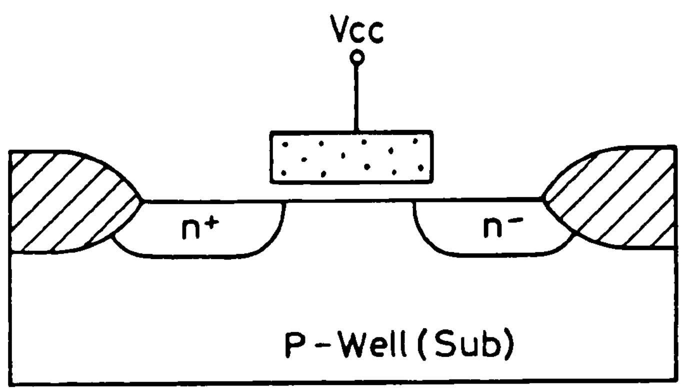


Fig. 7

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SELF-BOOTSTRAPPING DEVICE

The present invention relates to a self-bootstrapping device.

For example, the invention relates to a self-bootstrapping device for sufficiently bootstrapping a bias applied to the gate of a MOS transistor included in the decoder of a semiconductor memory device and requiring a high integration degree so that the MOS transistor can transmit the potential from its drain to its source.

Conventionally, self-bootstrapping devices have been used as decoders for decoding word lines of semiconductor memory devices in order to increase the integration of such semiconductor devices. Such self-bootstrapping devices also serve to boost an operating voltage to a level higher than the source voltage, thereby enabling word lines of memory devices to be effectively decoded.

NMOS transistors included in semiconductor memory devices, which may be those adapted to decode word lines or those included in pull-up drivers of data out buffers and coupled to the source voltage, need a gate potential higher than the sum of a drain potential and a threshold voltage.

It has been proposed to use a level shifter for boosting the potential at a particular node to a level considerably higher than the source voltage. However, with this method it is required to use a separate voltage supply source. Since the high level source voltage should be used at highly dense regions in this case, it may adversely affect the memory device. For example, the stability of the memory device may be degraded.

An alternative proposal uses two NMOS transistors, one of which acts to perform signal transmission. The other NMOS transistor is coupled to the gate of the signal transmission NMOS transistor. With such a construction, the signal transmission NMOS transistor has its gate voltage self-bootstrapped in accordance with variations in its drain voltage.

However, it is difficult to make the second NMOS transistor compact in proportion to the compactness of the signal transmission transistor due to various reasons involved in the fabrication thereof. As a result, there is a decrease in the bootstrapped voltage level.

It is an object of the invention to reduce the problems associated with the self-bootstrapping devices described above.

According to a first aspect of the present invention there is provided a transistor for use in a self-bootstrapping device comprising first and second diffusion regions formed in a semiconductor substrate; said first and second diffusion regions being spaced apart a predetermined distance; and a gate electrode formed over the semiconductor substrate between the first and second diffusion regions.

An embodiment of the invention when used in a self-bootstrapping device is capable of decreasing the capacitance of the junction capacitor in highly densely integrated semiconductor memory devices, thereby increasing the gate potential of the NMOS transistor used for signal transmission to a level higher than the sum of the drain potential and threshold voltage of the NMOS transistor.

In accordance with a further aspect, the present

invention provides a self-bootstrapping device including a first NMOS transistor for a signal transmission, and a second NMOS transistor connected between the gate of the first NMOS transistor and an address decoder circuit, the second NMOS transistor being applied at its gate with a source voltage, wherein the second NMOS transistor comprises; a first diffusion region formed at a required portion of a semiconductor substrate; a second diffusion region formed around the first diffusion region while being spaced apart from the first diffusion region by a desired distance; and a gate electrode formed over the semiconductor substrate between the first and second diffusion regions.

In accordance with a still further aspect, the present invention provides a self-bootstrapping device including a first NMOS transistor for a signal transmission, and a second NMOS transistor connected between the gate of the first NMOS transistor and an address decoder circuit, the second NMOS transistor being applied at its gate with a source voltage, wherein the second NMOS transistor comprises; a pair of diffusion regions formed in a semiconductor substrate while being spaced apart from each other by a desired distance, one of the diffusion regions being doped with impurity ions in a high concentration, and the other diffusion region being doped with impurity ions in a low concentration; and a gate electrode formed over the semiconductor substrate between the diffusion regions.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a circuit diagram illustrating a substantially conventional self-bootstrapping device;

Figure 2 is a circuit diagram illustrating another substantially conventional self-bootstrapping device;

Figure 3A is a plan view illustrating the layout of a boostrapping transistor used in conventional self-bootstrapping devices;

Figure 3B is a cross-sectional view taken along the line A-A' of Figure 3A;

Figure 4 is a plan view illustrating the layout of a self-bootstrapping transistor included in a self-bootstrapping device in accordance with a first embodiment of the present invention;

Figure 5 is a cross-sectional view taken along the line A-A' of Figure 4;

Figure 6 is a sectional view illustrating a self-bootstrapping transistor included in a self-bootstrapping device in accordance with a second embodiment of the present invention; and

Figure 7 is a sectional view illustrating a self-bootstrapping transistor included in a self-bootstrapping device in accordance with a further embodiment of the present invention.

NMOS transistors included in semiconductor memory devices, and used as self-bootstrapping devices to decode word lines or included in pull-up drivers, need a gate potential higher than the sum of a drain potential and a threshold voltage. A method proposed, which uses a level shifter for boosting the potential at a particular node to a level considerably higher than the source voltage, is illustrated in Figure 1 in which the level shifter is

denoted by the reference numeral 10. The level shifter 10 serves to boost the output from an address decoder circuit 20. A boosted signal from the level shifter 10 is applied to the gate of an NMOS transistor Q1. In this case, the boosted voltage Vpp output from the level shifter 10 should be higher than the maximum potential at the source or drain of the NMOS transistor Q1, namely, the source voltage Vcc, by a value corresponding to the threshold voltage. In this case, however, it is required to use a separate voltage supply source. Since the high-level source voltage should be used at highly dense regions in this case, it may adversely affect the memory device. For example, the stability of the memory device may be degraded.

In order to solve such problems, another scheme has been proposed, wherein a self-bootstrapping device is used. In this case, two NMOS transistors are used, one of which serves to perform a signal transmission. To the gate of the signal transmission NMOS transistor, the other NMOS transistor is coupled at its drain. With such a construction, the signal transmission NMOS transistor has a gate voltage self-bootstrapped in accordance with a variation in its drain voltage.

Such a self-bootstrapping device is illustrated in Figure 2. In this self-bootstrapping device, the signal transmission NMOS transistor, which may be that of Figure 1, is supplied at its gate with the drain voltage of the other NMOS transistor in place of an externally input particular voltage. In Figure 2, the NMOS transistor requiring the bootstrap is the transistor Q2. The other NMOS transistor Q3 is coupled at its source to the gate of the NMOS transistor Q2. The NMOS transistor Q3 is also coupled to an address decoder circuit 20. A gate capacitor C1 for the NMOS transistor Q2 is formed between the source and gate of the NMOS transistor Q2. A gate overlap

capacitor C2 is also formed between the gates of the NMOS transistors Q2 and Q3. A junction capacitor C3 is also formed because both the gate of the NMOS transistor Q2 and the source of the NMOS transistor Q3 have N^+ diffusion regions formed in a P^+ substrate, respectively.

Figure 3A illustrates the layout of a bootstrapping transistor used in substantially conventional self-bootstrapping devices. Figure 3B is a cross-sectional view taken along the line A-A' of Figure 3A. This transistor includes a pair of n^+ diffusion regions formed at desired portions of a semiconductor substrate and spaced apart from each other by a desired distance, and a gate electrode formed over the substrate between the n^+ diffusion regions.

The operation of the self-bootstrapping device having the above mentioned construction will now be described in conjunction with Figure 2. When the address decoder circuit 20 operates in response to an address input signal Ai applied thereto, it outputs a signal having a level corresponding to the source voltage Vcc. As a result, the NMOS transistor Q2 is applied at its gate with a voltage corresponding to the difference between the source voltage Vcc and the threshold voltage Vth. When the drain potential of the NMOS transistor Q2 increases up to an optional voltage Vx less than the voltage difference between Vcc and Vth, the gate potential of the NMOS transistor Q2 is self-bootstrapped by the capacitor C1 formed between the gate and source of the transistor Q2. As a result, the source potential of the NMOS transistor Q2 increases. At this time, the NMOS transistor turns off because the potential difference between its gate and source becomes lower than the threshold voltage.

In this case, the level of the self-bootstrapped voltage is determined by the co-relationship of the gate

overlap capacitor C2, the junction capacitor C3 and the gate capacitor C1 of NMOS transistor Q2. In other words, the self-bootstrapped voltage level is proportional to the value of $C1/(C1 + C2 + C3)$.

On the other hand, the NMOS transistor Q2 has a compact size when it is used in highly densely integrated semiconductor memory devices. In this case, however, the NMOS transistor Q3 is difficult to be compact in proportion to the compactness of the NMOS transistor Q2 due to various reasons involved in the fabrication thereof. As a result, the junction capacitor C3 has a relatively increased capacitance, as compared to the capacitor C1. This results in a decrease in the value of $C1/(C1 + C2 + C3)$, thereby dropping the bootstrapped voltage level of the NMOS transistor Q2.

Figure 4 illustrates the layout of a self-bootstrapping transistor included in a self-bootstrapping device in accordance with an embodiment of the invention. Figure 5 shows a cross-sectional view taken along the line A-A' of Figure 4.

As shown in Figures 4 and 5, the self-bootstrapping transistor has a drain 40 defined by an n^+ diffusion region formed at a desired portion of a semiconductor substrate. The transistor also has a source 50 disposed around the drain 40 but spaced apart from the drain 40 by a predetermined distance. The source 50 is defined by another n^+ diffusion region formed in the semiconductor substrate around the n^+ diffusion region of the drain 40 whilst being spaced apart from the latter n^+ diffusion region. The transistor further has a gate electrode 60 formed on the semiconductor substrate between the drain 40 and source 50. In order to minimise the size of the diffusion region of the drain 40, a single contact 30

having a minimum unit size, which is made of metal or polycide, is provided at the drain 40. The drain 40, source 50 and gate electrode 60 each has a rectangular or annular structure surrounding the contact 30.

Figure 6 is a sectional view illustrating a self-bootstrapping transistor included in a self-bootstrapping device in accordance with an alternative embodiment of the invention.

The self-bootstrapping transistor shown in Figure 6 has a drain 40' defined by an n^- diffusion region formed at a desired portion of a semiconductor substrate. A source 50' is disposed around the drain 40' but is spaced from the drain 40' by a predetermined distance. The source 50' is defined by an n^+ diffusion region formed in the semiconductor substrate around the n^- diffusion region of the drain 40' whilst being spaced apart from the n^+ diffusion region. The transistor also has a gate electrode 60' formed on the semiconductor substrate between the drain 40' and source 50'. Similar to the structure of Figure 5, a single contact, as 30, having a minimum unit size, which is made of metal or polycide, is provided at the drain 40' in order to minimise the size of the diffusion region of the drain 40'. The drain 40', source 50' and gate electrode 60' each has a rectangular or annular structure surrounding the contact 30.

In this embodiment, only the n^- diffusion region is used for a junction by use of a well known N^- MOS technique in which N^+ regions of a lightly doped drain (LDD) structure are masked. Accordingly, the junction capacitance resulting from N^+ diffusion regions formed in the substrate of P^+ type decreases. In the case of highly densely integrated circuits, accordingly, it is possible to efficiently self-bootstrap the gate potential of each MOS

transistor.

Figure 7 is a sectional view illustrating a self-bootstrapping transistor included in a self-bootstrapping device in accordance with a further embodiment of the invention.

The self-bootstrapping transistor shown in Figure 6 has an n^+ diffusion region and an n^- diffusion region both formed at desired portions of a semiconductor substrate while being spaced apart from each other by a predetermined distance. A gate electrode 60 is formed over the semiconductor substrate between the n^+ and n^- diffusion regions.

As apparent from the above description, the present invention provides an NMOS transistor having a self-bootstrapping function. The NMOS transistor can be fabricated using well known processing and fabricating techniques. The present invention reduces the junction capacitance resulting from N^+ diffusion regions formed in the P^+ substrate. In highly densely integrated circuits it becomes possible to efficiently self-bootstrap the gate potential of each MOS transistor.

It will be appreciated that various modifications, additions and substitutions may be made to the embodiments described and illustrated without departing from the scope of the invention as defined in the accompanying drawings.

CLAIMS

1. A transistor for use in a self-bootstrapping device comprising first and second diffusion regions formed in a semiconductor substrate; said first and second diffusion regions being spaced apart a predetermined distance; and a gate electrode formed over the semiconductor substrate between the first and second diffusion regions.

2. A transistor as claimed in Claim 1, wherein each of said first and second diffusion regions and said gate electrode is rectangular or annular in shape.

3. A transistor as claimed in Claim 1 or Claim 2, wherein only one pair of diffusion regions are formed in the semiconductor substrate and are spaced apart from each other by said predetermined distance.

4. A transistor as claimed in any preceding claim, wherein the transistor is an NMOS transistor.

5. A self-bootstrapping device comprising a first NMOS transistor for signal transmission and a second NMOS transistor for providing the gate voltage of the first transistor, wherein said second NMOS transistor is as claimed in any preceding claim.

6. A self-bootstrapping device comprising a first NMOS transistor for a signal transmission, and a second NMOS transistor connected between the gate of the first NMOS transistor and an address decoder circuit, the second NMOS transistor being applied at its gate with a source voltage, wherein the second NMOS transistor comprises:-

a first diffusion region formed at a required portion of a semiconductor substrate;

a second diffusion region formed around the first

diffusion region while being spaced apart from the first diffusion region by a desired distance; and

a gate electrode formed over the semiconductor substrate between the first and second diffusion regions.

7. A self-bootstrapping device as claimed in Claim 6, wherein the second NMOS transistor further comprises a contact formed at the first diffusion region.

8. A self-bootstrapping device as claimed in Claim 6 or Claim 7, wherein the first and second diffusion regions of the second NMOS transistor are doped with impurity ions in a high concentration.

9. A self-bootstrapping device as claimed in any of Claims 6 to 8, wherein each of the first and second diffusion regions and the gate electrode of the second NMOS transistor has a rectangular or annular structure.

10. A self-bootstrapping device as claimed in any of Claims 6 to 9, wherein the first diffusion region is doped with impurity ions in a low concentration, and the second diffusion region is doped with impurity ions in a high concentration.

11. A self-bootstrapping device as claimed in Claim 10, wherein the second NMOS transistor further comprises a contact formed at the first diffusion region.

12. A self-bootstrapping device as claimed in Claim 10 or Claim 11, wherein each of the first and second diffusion regions and gate electrode of the second NMOS transistor has a rectangular or annular structure surrounding the contact.

13. A self-bootstrapping device comprising a first NMOS

transistor for a signal transmission, and a second NMOS transistor connected between the gate of the first NMOS transistor and an address decoder circuit, the second NMOS transistor being applied at its gate with a source voltage, wherein the second NMOS transistor comprises:

a pair of diffusion regions formed in a semiconductor substrate while being spaced apart from each other by a desired distance, one of the diffusion regions being doped with impurity ions in a high concentration, and the other diffusion region being doped with impurity ions in a low concentration; and

a gate electrode formed over the semiconductor substrate between the diffusion regions.

14. A self-bootstrapping device substantially as hereinbefore described with reference to Figures 4 to 7 of the accompanying drawings.

The Patent Office

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Application No: GB 9526692.0
Claims searched: 1-14

Examiner: Miss J.E.Evans
Date of search: 22 February 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K (KDEG, KDES, KDEX)

Int Cl (Ed.6): H01L 29/78, 29/788

Other: ONLINE:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB2081012A	(Tokyo Shibaura Denki) see abstract & figs 2,4,5,14, and 15	1,3,6,8.
X	GB2033656A	(RCA) see abstract & fig 1	1,2,6,8,9, 12.
X	EP0463623A2	(Toshiba) see figs 1,5,6 and 9.	1,3,6,10, 13.

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